

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
 - a semiconductor substrate including a source region and drain region at its surface;
 - a gate electrode formed on said semiconductor substrate including a straight portion separating said source region and said drain region;
 - a dummy electrode formed at a position on an extension of a longitudinal direction of said straight portion on said semiconductor substrate;
 - a stopper insulating film, each overlying said gate electrode and said dummy electrode;
 - a sidewall insulating film covering a side of said gate electrode, said dummy electrode and said stopper insulating film;
 - an interlayer insulating film covering a top surface of said semiconductor substrate to cover up said sidewall insulating film and said stopper insulating film; and
 - a linear contact portion defined by a conductive member extending from vertically in said interlayer insulating film and electrically connected to one of said source region and said drain region at its bottom end, said linear contact portion being, when viewed from above, extending parallel to said straight portion of said gate electrode,
 - each longer side of a rectangle defined by said linear contact portion being, when viewed from above, located beyond said sidewall insulating film and within a top region of said gate electrode and said dummy electrode, and
 - a gap between said gate electrode and said dummy electrode appearing, when viewed from above, in said linear contact portion being filled with said sidewall insulating film such that said semiconductor substrate is not exposed.

2. The semiconductor device of claim 1, wherein said gate electrode is arranged in plurality parallel to each other and, when viewed from above, one of said source region and said drain region constitute a group of regions

5 of a specified type defined as regions between adjacent two of said gate electrodes being discrete linearly with an isolation insulating film therebetween, and said linear contact portion extends to integrally cover said group of regions of the specified type.

5 3. The semiconductor device of claim 2, wherein said one of said source region and said drain region is electrically connected, via said linear contact portion, to a first interconnection extending, above said linear contact portion, parallel to said straight portion, and the other of said source region and said drain region is electrically connected to a second interconnection extending, above said gate electrode, perpendicularly to said straight portion of said gate electrode.